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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**



Application Number: 10/603,327
Filing Date: June 25, 2003
Appellant(s): CHAMBLISS ET AL.

David W. Lynch (Reg. No. 36,204)
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 9/17/07 appealing from the Office action mailed 3/20/07.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 2003/0037178 A1 | Vessey et al. | 02-2003 |
| 2004/0205734 A1 | Tummalapalli | 10-2004 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

- Claims 31-48 and 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. No. 2003/0037178 A1 to Vessey et al.
- Claims 49,50 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,804,714 B1 to Tummalapalli in view of U.S. Pat. No. 2003/0037178 A1 to Vessey et al.

**Text of the Final Rejection**

Text of the Final Rejection is reproduced for convenience.

DETAILED ACTION

1. Claims 31-54 are pending in this application.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**3. Claims 31-48 and 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. No. 2003/0037178 A1 to Vessey et al.**

4. As to claim 31, Vessey teaches a program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform a method for providing a two-step communication scheme, the method comprising: establishing a portion of memory configured to provide asynchronous, connectionless inter-process communication between a first process and a second processes ("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460); granting exclusive access to a first process to the portion of memory configured to provide asynchronous, connectionless

("...without..." page 2 paragraph 0024) inter-process communication between the first process and the second process/while having been granted to the exclusive access to the portion of memory configured to provide asynchronous, connectionless inter-process communication, accessing the portion of memory configured to provide asynchronous, connectionless inter-process communication by the first process to modify the contents thereof to provide a message for processing by the second process ("...access right..." page 7 paragraph 0131, "...copies part..." page 17 paragraph 0237, "...Partition Ownership Mask...lock mechanism...acquire lock..." page 21 paragraphs 0287-0292, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307); and releasing exclusive access by the first process to the portion of memory configured to provide asynchronous, connectionless inter-process communication to prevent inter-process communication between the first and second process from becoming a performance bottleneck by releasing resources of the first process after the first process modifies the contents of the portion of memory ("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21 paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0348, page 27 paragraph 0360).

5. As to claim 32, Vessey teaches the program storage device of claim 31 further comprising configuring the memory to provide header having an operation code and a parameter region interpreted according to the operation code (figure 20 Control Structure header 1910 page 20 paragraph 0278, page 22 paragraph 0302-0304).

6. As to claim 33, Vessey teaches the program storage device of claim 31, wherein the providing the message into the portion of memory by the first process further comprises initiating a remote procedure call ("...procedural parameters..." page 21 paragraph 0278).

7. As to claim 34, Vessey teaches the program storage device of claim 31 further comprising granting exclusive access to the second process to the portion of memory configured to provide asynchronous, connectionless inter-process communication, while having been granted to the exclusive access to the portion of memory, accessing the portion of memory by the second process to modify the contents thereof to access the message provided in the portion of memory by the first process ("...lock mechanism...acquire lock..." page 19 paragraphs 0289-0292, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) and releasing exclusive access by the second process to the portion of memory page ("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21 paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0349, page 27 paragraph 0360).

8. As to claim 35,Vessey teaches the program storage device of claim 34 further comprising: establishing exclusive access to the portion of memory by the second process/accessing the portion of memory by the second process to provide a result

message in response to the message placed in the portion of memory by the first process ("...lock mechanism...acquire lock..." page 19 paragraphs 0289-0292, "...lock..." page 22 paragraph 0307); and providing by the second process a notification to the first process to check the portion of memory ("...inter-processor interrupt mechanism..." page 20 paragraph 0274, "...to alert..." page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send Signal..." page 26 paragraph 0349).

9. As to claim 36, Vessey teaches the program storage device of claim 31 further comprising providing by the first process a notification to the second process to check the portion of memory ("OS1 copies the offset pointer..." page 19 paragraph 0256, "...inter-processor interrupt mechanism..." page 20 paragraph 0274, "...to alert..." page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send Signal..." page 26 paragraphs 0349/0355).

10. As to claim 37, Vessey teaches a server comprising a memory (figures 22-24), wherein a portion of the memory is configured to provide two-step, asynchronous, connectionless inter-process communication between a first process and a second process, the portion of memory being configured as memory accessible by the first and second processes ("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460), wherein access to the portion of memory being granted exclusively to the first

process for modification of contents of the portion of memory to prevent inter-process communication between the first and second process ("... "exclusive window"..." page 6 paragraphs 0123/0128/0129, "...lock mechanism...acquire lock..." page 19 paragraphs 0289-0292, "...lock..." page 22 paragraph 0307) from becoming a performance bottleneck by releasing resources of the first process after the first process modifies the contents of the portion of memory ("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21 paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0349, page 27 paragraph 0360).

11. As to claims 38 and 42, see the rejection of claim 32 above.

12. As to claims 39 and 45, see the rejection of claim 33 above.

13. As to claim 40, Vessey teaches the server of claim 37, wherein the second process is granted exclusive access to the portion of memory configured to provide asynchronous, connectionless inter-process communication, accesses the portion of memory to modify the contents thereof to access the message provided in the portion of memory by the first process ("...lock mechanism..." page 19 paragraph 0289, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) and releases exclusive access by the second process to the portion of memory ("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21

paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0349, page 27 paragraph 0360).

14. As to claims 41, see the rejection of claims 35 and 36 above.

15. As to claims 42 and 48, see the rejection of claim 36 above.

16. As to claim 43, Vessey teaches a system (figures 22-24), comprising: a first process (OS1 2206a/APP1 2208a); a second process (OS1 2206n/APP1 2208n); and memory configured to provide asynchronous, inter-process communication between the first process and the second process, wherein the memory provides a portion of memory configured to be accessible by the first and second processes ("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460), wherein access to the portion of memory is granted exclusively to the first process for modification of contents of the portion of memory to prevent inter-process communication between the first and second process ("...lock mechanism...acquire lock..." page 21 paragraphs 0289-0292, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) from becoming a performance bottleneck by releasing resources of the first process after the first process modifies the contents of the portion of memory

("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21 paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0349, page 27 paragraph 0360).

17. As to claim 46, see rejection of claim 34 above.

18. As to claim 47, Vessey teaches the system of claim 46, wherein the second process is granted exclusive access to the portion of memory, accesses the portion of memory to provide a result message in response to the message placed in the portion of memory by the first process ("...lock mechanism...acquire lock..." page 21 paragraphs 0289-0292, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) and provides a notification to the first process to check the portion of memory ("...inter-processor interrupt mechanism..." page 20 paragraph 0274, "...to alert..." page 23 paragraph 0322, page 24 paragraphs 0328/0329, "Send Signal..." page 26 paragraph 0349).

19. As to claims 51-53, see the rejection of claim 1 above.

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**20. Claims 49,50 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,804,714 B1 to Tummalapalli in view of U.S. Pat. No. 2003/0037178 A1 to Vessey et al.**

21. As to claim 49, Tummalapalli teaches a service level agreement (SLA) server, comprising: a plurality of processes (figure 2 Col. 5 Ln. 25 – 67), the plurality of processes comprising a database manager for managing performance data, an application server for collecting performance data ("...concurrent processing server..." Col. 5 Ln. 45 – 65, Col. 7 Ln. 1 – 6) and providing a client interface for establishing service level agreements (User Layer tool 236/Service Reports tool 234 Col. 8 Ln. 45 – 53), a SLA core for analyzing data and controlling actions based on service level agreements and policy ("...concurrent processing managers..." Col. 5 Ln. 45 – 67, Col. 6 Ln. 66 – 67, Col. 7 Ln. 1 – 20) and a performance monitor daemon for communicating with remote I/O service gateways to collect data and send throttling requests ("Database performance monitor..." Col. 6 Ln. 42 – 59);

Tummalapalli is silent with reference to memory configured to provide asynchronous, inter-process communication between the processes, wherein the memory provides a portion of memory configured to be accessible by the processes, wherein access to the portion of memory is granted exclusively to a first of the

processes for modification of contents of the portion of memory to prevent inter-process communication between the process from becoming a performance bottleneck by releasing resources of the first of the processes after the first of the processes modifies the contents of the portion of memory.

Vessey teaches a memory configured to provide asynchronous, inter-process communication between the processes, wherein the memory provides a portion of memory configured to be accessible by the processes ("...shared memory...memory region..." page 2 paragraphs 0024-0028, "...shared memory window..." Main Memory 160 page 5 paragraph 0109, page 6 paragraphs 0121/0130, page 17 paragraphs 0236/0237, page 18 paragraph 0240, page 20 paragraph 0274, figures 22/23 Shared Memory 160, figure 34 Shared Memory 3460), wherein access to the portion of memory is granted exclusively to a first of the processes for modification of contents of the portion of memory to prevent inter-process communication between the process ("...access right..." page 7 paragraph 0131, "...copies part..." page 17 paragraph 0237, "...lock mechanism...acquire lock..." page 19 paragraphs 0289-0292, "...updating information..." page 23 paragraph 0319, "...lock..." page 22 paragraph 0307) from becoming a performance bottleneck by releasing resources of the first of the processes after the first of the processes modifies the contents of the portion of memory ("...Partition Ownership Mask...lock mechanism...DeallocationLock field..." page 21 paragraphs 0287-0292, "Deallocate Shared Memory..." page 26 paragraph 0349, page 27 paragraph 0360).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Vessey and Tummalapalli because the teaching of Vessey would improve the system of Tummalapalli by providing a locking mechanism for locking shared memory in order to facilitate greater throughput between partitions, since contention for system lock is eliminated (Vessey page 22 paragraph 0307).

22. As to claims 50 and 54, see the rejection of claim 49 above.

**(10) Response to Argument**

Appellant argues in substance that (1) the Vessey prior art reference teaches away from the invention by not teaching connectionless inter-process communication but rather allow connection between its first and second partitions and therefore maintaining connection that tie tying up finite resources, and (2) the Vessey prior art reference does not teach or suggest allowing exclusive access to shared memory by a partition and does not teach or suggest releasing exclusive access by a first process to a second process which then obtain exclusive to the same portion of memory and change the contents of the portion of memory.

Examiner respectfully traverses Appellant's arguments:

As to point (1), the Vessey prior art reference discloses a process for emulating network communications between applications executing in different partitions of a partitionable computer system. A connection is established between a first partition and

a second partition of a computer system, through a memory region of the computer system shared by both the first partition and the second partition. The connection emulates a network connection through application programming interface. A network message is transmitted from a first application in the first partition using a network application interface and intended for transmission to a second application in the second partition. The network message transmitted by the first application is transmitted to the second application via the connection established through the shared memory region. By emulating network communications between partitions via application programming interface and shared memory the use of an external network between the partitions is eliminated (page 2 paragraph 0024) and therefore negates Appellant's assertion that the Vessey prior art reference does not teach connectionless inter-process communication.

As to point (2), as indicated above the network message transmitted by the first application is transmitted to the second application via the connection established through the shared memory region. The Vessey prior art reference also discloses a lock mechanism implemented through a (Core Services software) that allows different applications/partitions to lock access to various memory structures of the shared memory region as needed to ensure that **only one application/partition is capable of modifying any memory structure at a given time** (page 21 paragraph 0289) during the network message transmission process. Before using the shared memory region, the sending application (first application or first partition) must first, using the locking mechanism, allocate and lock part of the shared memory region (allowing exclusive

access to shared memory) needed for transmitting the network message (page 25/26 paragraphs 0347/0354/0356, page 27 paragraph 0360). After allocating and locking part of the shared memory region the sending application fills/populates the allocated shared memory region with data/information for transmission to the receiving/second application/partition. As for releasing exclusive access by a first process, the lock mechanism via the (Core Services software) interface (Deallocate Shared Memory) allows a client (sending/first application/partition) to request for the de-allocation of part of shared memory region that it had earlier acquired lock to (page 26 paragraph 0348, page 27 paragraphs 0360/0366). The locking mechanism as taught by the Vessey prior art reference therefore contradicts Appellant's assertion that the Vessey prior art reference does not teach steps or process of allowing exclusive access and subsequently releasing the exclusive access.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

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